Chip Scale Package Implementation Challenges

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ABSTRACT

The JPL-led MicrotypeBGA Consortium of enterprises representing government agencies and private companies have jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. In the process of building the Consortium CSP test vehicles, many challenges were identified regarding various aspects of technology implementation. This paper will present our experience in the areas of technology implementation challenges, including design and building both standard and microvia boards, and assembly of two types of test vehicles. We also discuss the most current package isothermal aging to 2,000 hours at 100°C and 125°C and thermal cycling test results to 1,700 cycles in the range of –30 to 100°C.

CSP IMPLEMENTATION CHALLENGES

Emerging CSPs are competing with bare die assemblies and are becoming the package of choice for size reduction applications. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages.

Two concepts of CSPs are shown in Figure 1. The concepts presented include: (1) Grid CSPs with wire bond and C4 (Control Collapse Chip Connection) technology (rigid or flex interposers), and wafer level molding assembly and redistribution, and (2) Leaded and no leads (leadless) for low I/O applications.

In the process of building the JPL-led consortia test vehicles [1], numerous challenges were identified. The thought processes for the first test vehicle started in late 1996, when very few packages were available for evaluation. The design for the second test vehicle initiated in mid 1998, when a much larger number of CSPs were available, estimated to be nearly fifty types. Although CSPs' rapid growth has eased package availability, its implementation, especially for high reliability applications, requires establishment of many technical issues including assurance for quality and confidence in reliability, as well as development of the necessary infrastructure.

In the following, key challenges for package and PWB design, and assembly of test vehicles will be presented. Also, the most update environmental test results for package and assemblies will be reviewed.

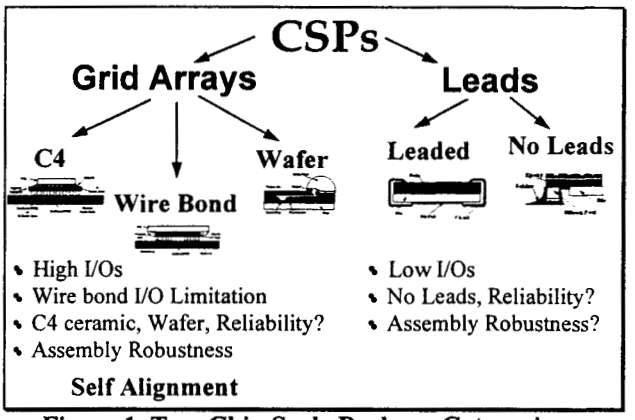


Figure 1 Two Chip Scale Package Categories

Confusion on CSP Definition

Although the expression of CSP is widely used by industry from suppliers to users, its implied definition had evolved as the technology has matured. At the start of the package's introduction into market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package. A rapid transition to a much lower size was difficult both by package suppliers and end user. Suppliers had difficulty in building packages with such a definition whereas the users had difficulties with accommodating the need for the new microvia printed circuit board (PWB) because of routing requirement and its increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using standard PWB design rather than the microvia build to avoid cost.

The "expert definition" undermines one of the key purpose of the package allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the

footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

Therefore, CSPs are miniature new packages that industry is starting to implement and there are many unresolved technical issues associated with their implementation. For example, in early 1997, packages with 1mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. Other changes included the use of flip chip die rather than wire bond in CSP.

Package Availability in Early 1997

CSP's availability in daisy chain for the attachment reliability characterization was one of the challenging issues at the start of the program in early 1997. There were numerous publications on a wide range of CSPs, but most packages were in early development and lacked package reliability information. Assembly reliability data were even rarer. Most packages were only available in prototype form, and this, of course, did not guarantee the package similarity to the production version or even their future availability.

More than a six month delay in package delivery date was the norm. Four packages dropped from the program, and one was delayed almost a year with last moment modification by supplier. Although many suppliers promoted their packages and package reliability, they were not willing to submit their packages for an independent evaluation, possibly because of lack of confidence.

Numerous packages from leaded and leadless to grid CSPs were chosen for evaluation. At the start of program, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O, 0.5mm package, was dropped by the manufacturer prior to the trial test vehicle assembly. Therefore, the maximum I/O package now is a CSP with 275 I/Os. Three other higher I/O with 0.5mm pitch were also dropped prior to full build. A hard metric, 0.5mm, CSP package with 188 I/O with data given by supplier for the English pitch version, was among these three packages. The supplier was unable to meet our last build schedule, late in 1998. These trends clearly indicated that the package suppliers were struggling to build CSPs with 0.5mm, especially with high I/O counts.

The majority of the next phase of the CSP program have pitches of 0.8mm. In this phase, there are a few high I/O CSPs with 0.5mm pitch. This indicates that industry is starting to be more comfortable with moving towards a tighter pitch at higher I/O.

Lack of Design Guidelines

Guidelines and standards on various elements of CSPs were not available. For example, there was missing package daisy chain information, and insufficient mechanical drawing data to begin with. The majority of packages were hard metric, however, a few with the inch pitches caused dimensional errors when converted from inch to metric. Furthermore, ball and pad information needed for board design was missing and it was time consuming to gather information from suppliers since most needed to be generated by technical personnel. There was no information on pad design relative to package pad for achieving optimum reliability. Pads for PWBs could be assumed to be the same as package, as a rule of thumb. For our design, guidelines developed by the package suppliers were used when available. Otherwise, available knowledge and engineering judgment were utilized.

Need for Microvia PWB

The standard PWB design could be used for low I/O CSPs. Build up (microvia) board technology is required for higher I/O CSPs in product with active die. For daisy chain packages, it is possible to design high I/O on a standard board. Board design guidelines are needed, especially for the build up (microvia) configuration.

I/O Limitation

There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM (surface mount) packages, direct chip attachment (DCA), BGAs, and CSPs on one board is another expected design and assembly challenge. This mixed technology is being considered for the next test vehicle under the second JPL-led CSP Consortium.

CSP Test Vehicle Design

The Consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

Package — Ten packages from 28 to 275 as listed in Table 1. The TSOP was used as control.

Printed Wiring Board (PWB) Materials and Build — Both FR-4 and BT (Bismaleimide Triazine) materials were available in the resin copper coated form for evaluation. High temperature FR-4 and Thermount® were also included. The boards were double sided, standard and microvia. With our design, direct reliability comparison between the two board

technologies as well as double side processing is possible. In designing daisy chains, it became apparent that the standard PWB technology could not be used for routing the majority of packages.

Table 1 CSP Package Configurations Matrix

Package ID	Package. Type	Package Size Mm	Pad Size mm	Pitch mm	I/O Count	Package. Thickness mm	Ball Diam mm
A	Low I/O Wafer	1.6 x 3.2	0.25 x 0.15	0.5	12	0.5	0.075
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	96	1.75	0.3
H	CSP-Redistribution-1	10.025 x 8.995	0.254	0.5	96	-	0.3
I	CSP Redistribution-2	6.22 x 5.46	0.254	0.5	99	-	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
L	TAB CSP-3	13.1 x 13.1	0.3	0.5	188	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	225	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

* All measurements are in mm unless otherwise specified

Daisy Chain — Packages had different pitches, solder ball volumes and compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes were developed.

Surface finish — At least four types of surface finishes were considered. Organic solder preservative (OSP), hot air solder leveling (HASL), Au/Ni (two thicknesses), and immersion silver; the majority were OSP finish. Three types of solder pastes were included: no-clean, water soluble (WS), and rosin mildly activated (RMA).

Underfill — Packages with underfill requirements were included both with and without underfill to better understand the reliability consequence of not using underfill.

Double Sided Assembly — PWBs were double sided and several boards with double sided packages were assembled to investigate the reliability of single sided versus double sided test vehicles, as well as standard versus microvia technology.

Solder Volume — Three stencil thicknesses were included: high, standard, and low. The two extreme thicknesses were 4 and 7 mils with different stencil aperture design depending on the pad size. The standard which was used for the majority of test vehicles was 6 mil thickness.

Test Vehicle Feature — The test vehicle was 4.5 by 4.5 inches and divided into four independent regions. For single side assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages. All packages were daisy chained and they had up to two internal chain patterns.

Environmental testing — To link our data to those generated for Ball Grid Array, two conditions of -30 to 100°C (A cycle) and -55 to 125°C were included. The A cycle profile is shown in Figure 2. There are other cycling conditions that have yet to be defined. For example, thermal cycling will be performed between 0 and 100°C to meet the needs of commercial team members. In addition, mechanical vibration and shock

will be performed and theoretical modeling will be carried out as needed.

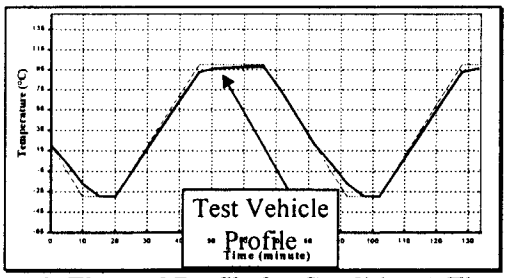


Figure 2 Thermal Profile for Condition A Thermal Cycling (-30°C to 100°C)

ISOTHERMAL AGING CSP/BGA

This investigation included isothermal aging of BGA as well as grid CSP packages to determine degradation of ball/package with temperature and time as well thermal cycling. Other objectives were to determine if there were differences in package/ball interface integrity for different package before and after isothermal exposure and if this correlated with cycles to failure test results. The isothermal temperatures were the maximum thermal cycling temperatures.

BGA Assembly Failure From Ball/Package

For BGA, failures either between ball and package or ball and PWB (solder joint) were observed after thermal cycling. For grid CSPs, the interface between package and solder balls is also a potential failure site.

For BGAs, cycles to failure and failure mechanisms under different environments were investigated under another program [2,3]. Figure 3, adapted from Reference 3, shows cumulative failure percentages versus increasing cycles for several plastic BGA assemblies. Wider distribution for two peripheral BGA packages can be seen in this figure.

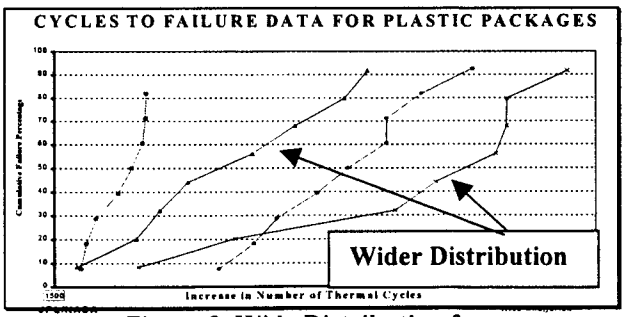


Figure 3 Wide Distribution for Two BGA Package Types

The exact causes of wider distributions are yet to be identified. Possible causes include: PWB materials (FR-4, polyimide), solder volume, and ball/package metallurgy/integrity. Package/ball integrity plays a role since failure analyses of cycled BGA assemblies indicated that failures occurred either at package or board interfaces. In addition, up to a 50% reduction in strength was found when another type of BGA build was subjected to isothermal aging for 1,000 hours at 125°C. It is not known if this large reduction was an exception because of build configuration or if it would be true for other widely used BGA configurations.

Test Procedures

Both plastic and ceramic BGAs, with their thermal cycling behavior already characterized, were subjected to shear testing before and after isothermal aging exposure. The grid CSPs were from the Table 1 list.

Both BGA and CSP packages were subjected to visual inspection and scanning electron microscopy (SEM) to characterize their joint quality, solder ball metallurgy, and elemental compositions. In addition, several assemblies from a grid CSP were subjected to pull tests before thermal cycling and after at 1,500 cycles (-30 to 100 °C).

Ball Shear Prior to Isothermal Aging

Figure 4 shows as-received cumulative percentage versus shear forces for various BGAs and grid CSPs. The median ranking (i-0.3/n+0.4) was used to calculate cumulative percentages. The fifty percentile shear forces as well as their respective shear stresses are shown in Table 1.

Shear forces ranged from 170 to about 400 grams for CSPs and from 1,000 to 1,500 grams for plastic and ceramic BGAs. Shear force depends on many variables including the pad size, metallurgy, and configuration attachment as well a chemistry of solder. Shear force values become critical with mechanical conditions.

Shear stresses were calculated based on the sheared surface areas and had a much narrower range for both CSPs and BGAs. They ranged from 3.8 to 5.7 kgrm/mm^2 except for a grid CSP with value of 7.6 kgrm/mm^2. This might be due to solder metallurgy as well as ductile failure during shear testing.

It is interesting to note the significant difference in shear forces for different packages. Distributions for the same packages from different suppliers were slightly different. The CSP-2 with non clearance mask had a tighter force distribution.

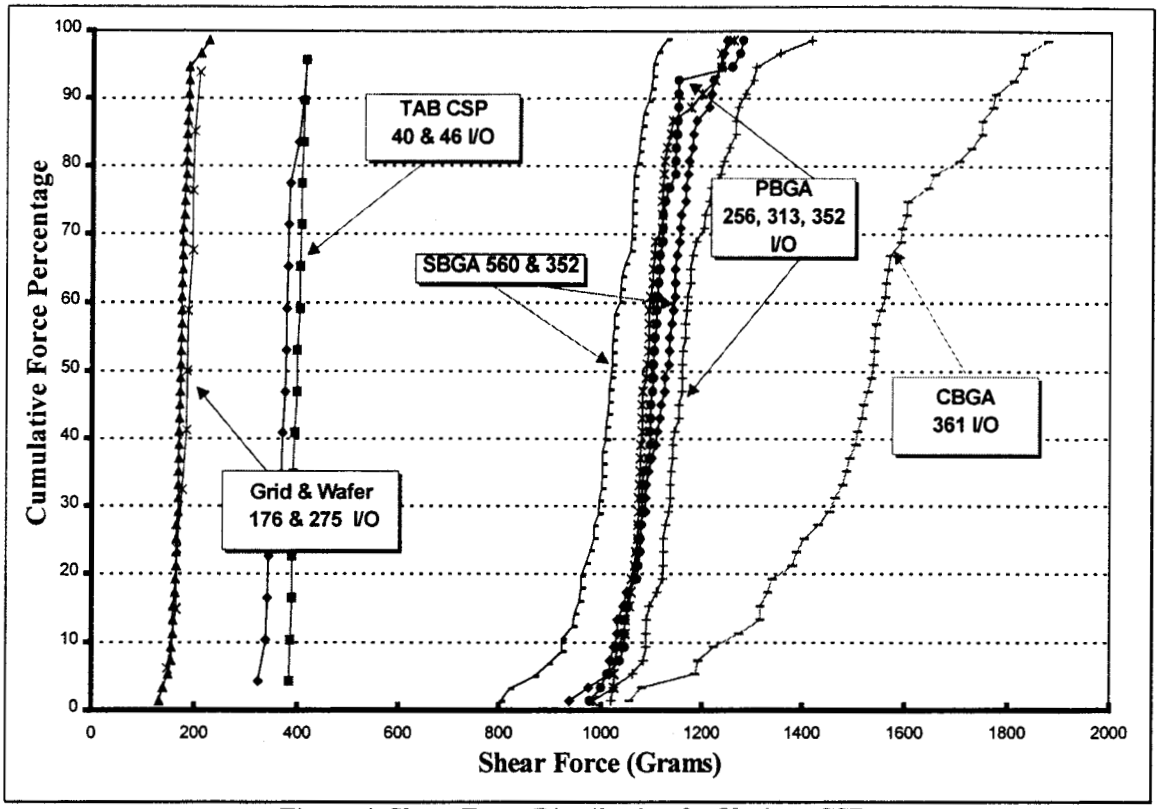


Figure 4 Shear Force Distribution for Various CSPs

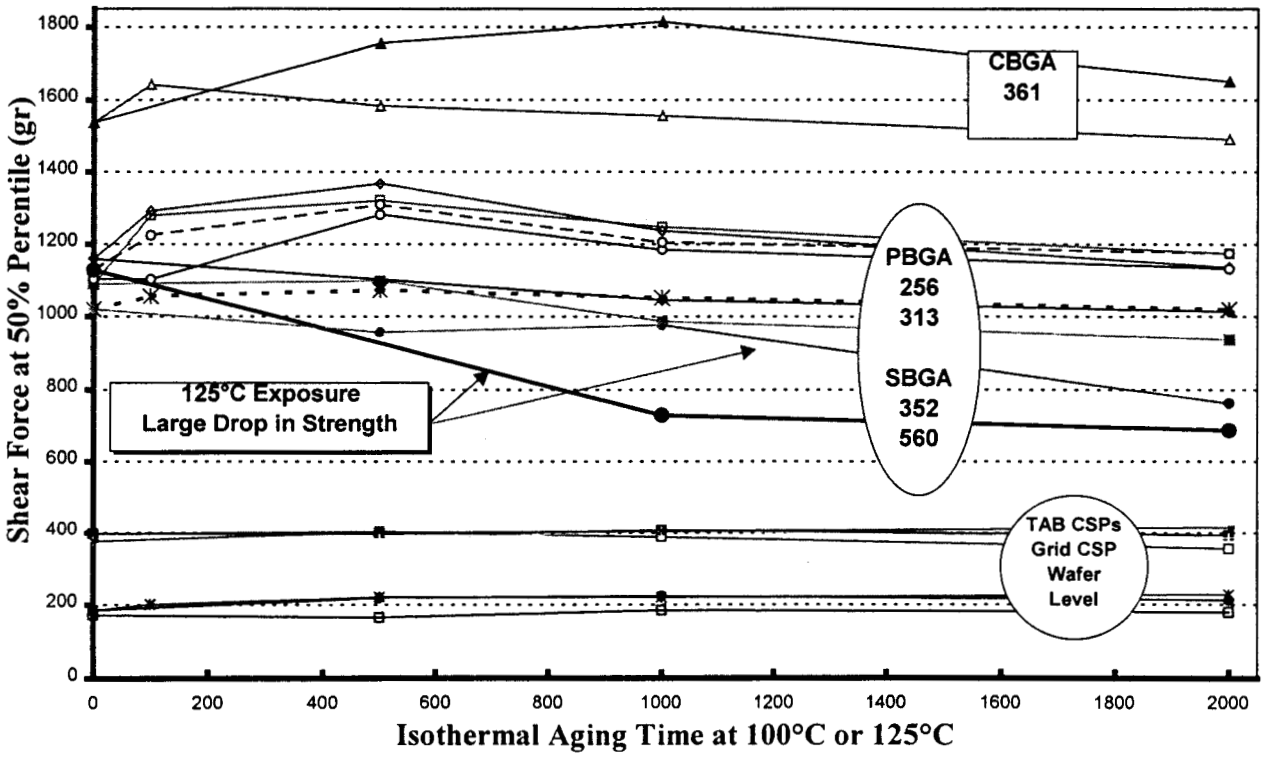
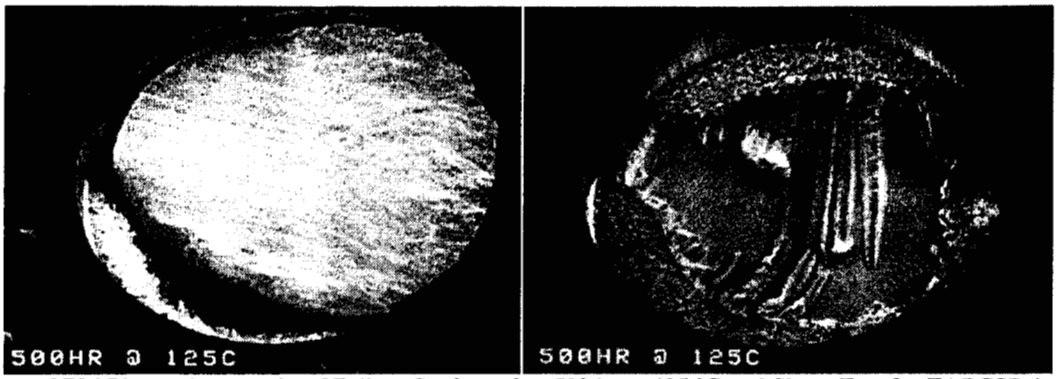
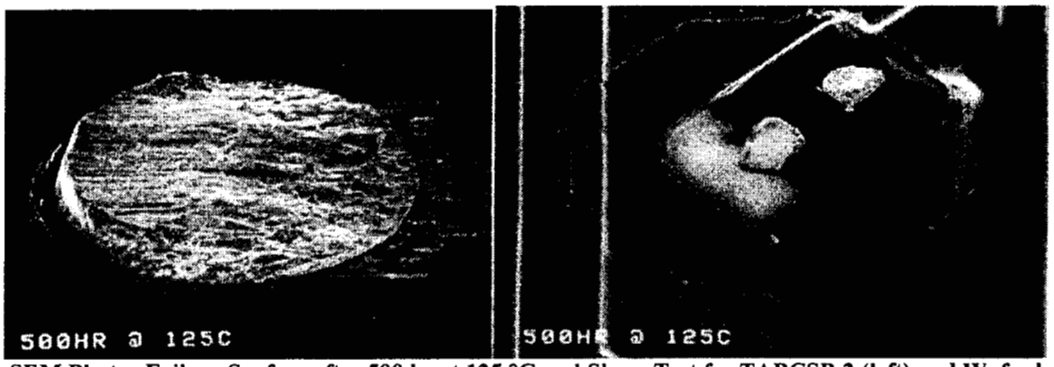


Figure 5 Ball/Package Shear Forces (N50%) vs. Time for Isothermal Aging at 100 and 125 °C for a Number of CSP and BGA Packages



(a) SEM Photomicrographs of Failure Surface after 500 hr at 125 °C and Shear Test for TABCSP-1



(b) SEM Photos Failure Surface after 500 hr at 125 °C and Shear Test for TABCSP-2 (left) and Wafer level

Figure 5 SEM Photos of Failure Surface after Isothermal Aging Various CSPs

Isothermal Aging

Figure 5 shows the 50% shear force values (N50%) for both BGA and CSP packages tested at 100 and 125°C to 2,000 hours. There are three distinct regions: CSPs, PBGAs, and CBGAs. In general, irrespective of package types, shear forces increased with aging initially and dropped slightly at higher aging times.

Shear data without the record of failure mechanism might be of no value. For example, the wafer level package showed improvement after exposure. The most probable cause of improvement after exposure at 100°C is microstructural changes which could have reduced the processing residual stresses. However, improvement after exposure at 125°C is meaningless, since shearing was a mode change from ball/package interface failure to tearing after exposure due to significant degradation of package build up (see Figure 6).

The two SBGA packages showed a different trend. Shear forces decreased with increasing aging times and about 40% dropped after 1,000 hours. Assemblies for both BGAs had wide distribution. The widest distribution was for PBGA 256 having the same trend as other BGAs.

ASSEMBLY

The Consortium assembled thirty #1 test vehicles (TV) and seven trial #2 test vehicles. Ball grid arrays are known to be robust in manufacturing, but there is disagreement on the acceptable manufacturing offsets for CSPs. No defects were observed when thirty #2 test vehicles, each with 4 grid CSPs with 46 I/Os, were assembled.

Quality of Solder Joints

Figure 7 shows a SEM photomicrograph of a solder joint for a TAB CSP and a low I/O wafer level (8 I/O) package on a board for #1 TV. Low package height made inspection of the joints very difficult, either by visual or by SEM. Three of these wafer packages showed poor quality solder joints with signs of cracking. Poor quality of the package was the reason for existence of microcracks after assembly. For these reasons, this package was excluded for the #2 test vehicle assembly.

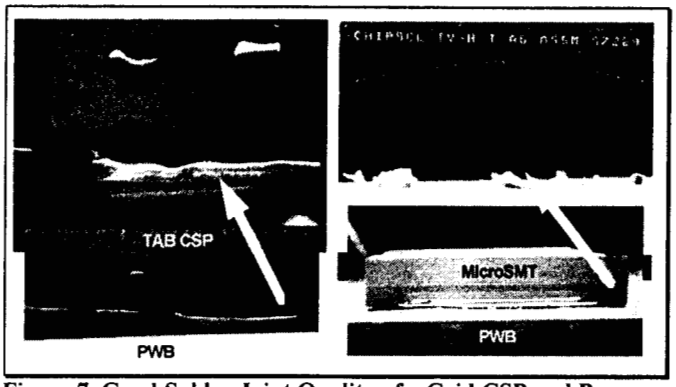


Figure 7 Good Solder Joint Quality of a Grid CSP and Poor Solder Joint Quality of Low I/O Wafer Level

PULL TEST- AS ASSEMBLED

Four of the TAB CSP-1 assemblies (#1 TV) were subjected to pull test after assembly prior to other environmental tests. The tensile loads were recorded for comparison and detached board/package surfaces were inspected for the failure mechanism. The following was found:

- No solder joint failures were observed; failures were at ball/package traces.
- The tensile forces for four assemblies were: 28, 25, 22, and 13 lb. The 13 to 28 lb. for a package of 46 I/Os is equivalent to 128 to 247 g/ball. Shear forces for the same package before exposure to reflow process ranged from 320 to 400 g/ball (see Table 1).

PULL TEST- AFTER THERMAL CYCLING

A number of the assembled test vehicles were subjected to thermal cycling. The cycle ranged from -30 to 100°C and had an increase/decrease heating rate of 2 to 5°C/min and dwell of about 20 minutes at the maximum temperature, to assure near complete creeping. The duration of each cycle was 82 minutes. The CSP packages had internal daisy chains which made a closed loop with daisy chains on the PWB, enabling the monitoring of solder joint failures through interval electrical resistance measurement. Measurements were performed at room temperature on assemblies removed from the thermal cycling chamber. Cycles to failure were recorded.

After 1,500 cycles, several TAB CSP-1 assemblies were subjected to pull testing to determine strength degradation due to thermal cycling. In addition, failure sites and damaged areas were identified by using die penetrant prior to tensile test. The tensile loads for four test vehicles, each with four packages, are listed in Table 2.

Tensile loads for thermally cycled TVs ranged from 14 to 25 lb. force which are similar to the assembled tensile test results. No significant decrease in tensile strength indicates that solder joints had minimal degradation due to 1,500 thermal cycles.

Balls failed at ball/package interface within traces. There was no presence of dye penetrant on the fractured surfaces, i.e. no solder joint failures. This is a clear indication that failure due to thermal cycling, evident by the daisy chain opens for three assemblies, occurred within the package rather than in solder joints as commonly observed after thermal cycling.

No attempts were made to narrow the internal failure site since other investigators have identified the failure types for this package [4]. Failures have been reported to be from the TAB lead bond. Package internal failure might be true only for those fabricated from an early production version which were used in this test vehicle. This was verified by comparing the serial number on the package with the package supplier data base. The #2 TV includes packages from a more recent production version. This will help determine if indeed improvement in cycles to failure can be achieved by the new modified TAB lead bond version.

Table 2 Tensile forces before and after thermal cycling (1500 cycles, -30/100°C)

TAB CSP-1 46 I/O	Tensile Force As Assembled (lb force)	Tensile Force After 1,500 For 4 TVs (lb force)
A site	13	17,25,24*,23
B site	22	22,18,14,25*
C site	25	?,23*,18,20
D site	23	22,18,15,20
* Daisy chains were open at 1,500 cycles		

THERMAL CYCLING TEST RESULTS

Seven trial #2 test vehicles were assembled to optimize the assembly process and profile. The lowest stencil thickness, 4 mil, was used to determine the worst condition, that is, solder starving condition on a leadless package. A stencil thickness of 6 mil is the recommended thickness for assembly of leadless packages. One test vehicle was assembled double sided. Five of the PWBs had OSP surface finish, and two had HASL. All PWBs including the PWBs with HASL finish, were successfully assembled. As expected, working with HASL was much more difficult than OSP.

The five trial test vehicles with the OSP finish were subjected to thermal cycling in the range of -30 to 100°C (A condition). Both PWB and assembly conditions were not optimum for the trial test. Therefore, thermal cycling results may well suggest potential areas where the process can be optimized for the production test vehicle assemblies. Results are not valid for reliability and

failure statistic analyses because of the low number of test samples and non-optimum condition.

For the trial test vehicle, automatic monitoring was impossible since connections to the ground plane were missed during file translation for PWB fabrication. This was corrected. For the full production assemblies, these daisy chains will be monitored continuously. For trial test vehicles, resistances were measured manually before and at different thermal cycling intervals to check for electrical opens (solder joint failure).

Table 3 shows resistances before and at different thermal cycles to 1,700 cycles. A number of assemblies were removed at different cycles for cross-section examination. Assemblies were periodically removed from the chamber and checked at room temperature (RT) for resistance (Ω). The word "Open" in the Table indicates electrical open at RT and the word "STOP" indicates cycling discontinuation on the TV. Resistances are different for different daisy chain patterns, but are approximately the same for the same package on various test vehicle assemblies. It is interesting to note that even for non-optimum conditions, the majority of solder joint assemblies survived to 700 cycles with only two exceptions.

Table 3 Daisy Chain Resistances of Assembled CSPs at Various Number of Cycles at Condition A (-30/100°C)

Package ID	Pkg ID	Pkg ID	Cycles 0	Cycles 100	Cycles 300	Cycles 400	Cycles 500	Cycles 600	Cycles 700	Cycles 900	Cycles 1000	Cycles 1200	Cycles 1500	Cycles 1700
Leadless-1	B	22-μvia	2.8	2.8	Open	Open	Open	Open	Open	Open	Open	Open	Open	STOP
Leadless-2	E	22-μvia	4.6	4.7	5.4	4.8	4.8	4.8	4.9	4.9	4.7	4.4	4.4	STOP
TAB CSP-1	F	22-μvia	9.3	9.2	9.5	9.3	9.4	9.5	9.6	9.4	9.5	9.1	9.2	STOP
TSOP 46 I/O	D	22-μvia	6.8	6.6	7	6.8	6.8	6.6	6.8	6.9	6.6.	6.7	6.5	STOP
TAB CSP-2	C	22-μvia	5.8	5.7	6	6.2	5.7	5.9	5.8	5.9	5.7	5.7	5.6	STOP
Wafer Level	O-1	22-μvia	20.9	20.7	21.2	21.1	21.2	21.1	21.2	21.1	20.6	20.6	20.9	STOP
Wafer Level	O-2	22-μvia	23.7	23.5	23.8	23.7	23.6	23.7	23.8	23.9	23.4	23.3	23.4	STOP
Leadless-1	B	22-STD	2.3	2.3	2.6	2.7	2.6	2.4	Open	Open	Open	Open	Open	STOP
Leadless-2	E	22-STD	4	4.1	4.1	4.3	4.2	4.1	4.2	4.2	4	4.1	Open	STOP
TAB CSP-1	F	22-STD	9.3	9.3	9.4	9.4	9.2	9.2	9.6	9.6	9.5	9.1	9.2	STOP
TSOP 46 I/O	D	22-STD	5.9	6.3	5.9	6.2	5.8	5.8	6.2	6	6.1	5.8	5.7	STOP
TAB CSP-2	C	22-STD	6.1	6.2	6.9	6.6	6.9	6.3	6.6	7.1	45.8	1.4k	Open	STOP
Wafer Level	O-1	22-STD	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	STOP
Wafer Level	O-2	22-STD	28.6	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	STOP
Leadless-1	B	29-STD	2.8	2.8	2.9	3	2.9	2.8	2.7	Open	Open	STOP	STOP	STOP
Leadless-2	E	29-STD	4.6	4.8	5.1	4.9	4.9	4.8	4.8	4.8	5	STOP	STOP	STOP
TAB CSP-1	F	29-STD	9.7	9.6	9.6	9.7	9.7	9.6	9.7	9.7	9.6	STOP	STOP	STOP
TSOP 46 I/O	D	29-STD	6.7	6.8	7	7	6.8	7	7	7	7	STOP	STOP	STOP
TAB CSP-2	C	29-STD	5.6	5.7	5.7	5.6	5.7	5.7	5.7	5.7	5.8	STOP	STOP	STOP
Wafer Level	O-1	29-STD	21.6	21.6	21.7	21.8	21	21.6	21.6	21.9	21.7	STOP	STOP	STOP
Wafer Level	O-2	29-STD	24.5	24.6	24.6	24.7	23.5	24.8	24.7	24.7	24.4	STOP	STOP	STOP
Leadless-1	B	3-STD	2.8	2.8	2.9	2.9	2.9	2.6	2.7	3	2.7	2.7	3	Open
Leadless-2	E	3-STD	4.7	4.7	4.9	5.1	4.8	4.7	4.8	4.9	4.7	4.5	4.7	4.1
TAB CSP-1	F	3-STD	9.5	9.4	9.6	9.7	9.6	9.8	9.5	9.8	9.7	9.9	9.6	9.2
TSOP 46 I/O	D	3-STD	6.8	6.7	7	7	7.1	6.9	6.9	7.5	7.1	6.7	6.6	6.7
TAB CSP-2	C	3-STD	5.7	5.6	6	5.9	5.9	5.6	5.9	210	58.6	1.4k	Open	Open
Wafer Level	O-1	3-STD	19.2	19.1	19.4	19.2	19.8	19.1	19.5	19.6	19.3	19	19	Open
Wafer Level	O-2	3-STD	22.8	22.6	22.9	22.9	22.7	22.6	23	23.1	23.3	22.6	Open	Open
Leadless-1	B	19-STD	2.8	2.7	2.9	3.2	2.9	STOP	STOP	STOP	STOP	STOP	STOP	STOP
Leadless-2	E	19-STD	4.8	4.7	5	4.6	4.7	STOP	STOP	STOP	STOP	STOP	STOP	STOP
TAB CSP-1	F	19-STD	10	10	10.1	10.3	10.6	STOP	STOP	STOP	STOP	STOP	STOP	STOP
TSOP 46 I/O	D	19-STD	6.8	6.8	6.9	6.7	6.5	STOP	STOP	STOP	STOP	STOP	STOP	STOP
TAB CSP-2	C	19-STD	7.8	Open	Open	Open	Open	STOP	STOP	STOP	STOP	STOP	STOP	STOP
Wafer Level	O-1	19-STD	23.3	23.3	23.3	23.7	24.7	STOP	STOP	STOP	STOP	STOP	STOP	STOP
Wafer Level	O-2	19-STD	24.8	24.7	24.8	25	23.3	STOP	STOP	STOP	STOP	STOP	STOP	STOP

The first exception was for the wafer level package (22-STD) with failure between 0 and 100 cycles. No underfill was used. This package is known to require underfill and those which were underfilled survived to 1500 thermal cycles.

The second exception was for the leadless package (22-μvia) which failed between 100 and 300 cycles from the μvia side. This package was mounted on a double sided assembly (22-STD and 22-μvia) with the microvia side (22-μvia) reflowed first, i.e, these joints were exposed to two reflows. In an effort to determine the cause of this early failure, it was also noticed that this is the only package that exactly overlapped another leadless package in the second side with a 90 degrees rotation. The lay out for the double sided assembly was not mirror imaged. One image was rotated 90 degree relative to the first image.

During visual examination, it was noticed that the first failure location was at two cross-over corners. The criticality of solder disturbance at the crossing corners will be verified in testing of the full production test vehicles. Early joint failure for double sided assemblies is qualitatively in agreement with another investigators' test results [5]. It was reported that a reduction of almost 50% in cycles to failure for double sided assemblies was seen with the mirror imaged packages. The number of cycles-to-failure was increased as double sided package assemblies moved away from the mirror position.

The other failures of 22-STD (O-1), and 19-STD, were considered to be defect related, including package and PWB. The O-1 package was from the preproduction and provided for assembly purpose only. Via misregistration and solder mask coverage on the pads are other potential source of early failure.

Recall that these test vehicles were from the trial run, the chief purpose of which was to understand the critical issues of PWB fabrication, process optimization, and daisy chain verification. Currently, a large number of TVs from the 150 full production assemblies are being thermally cycled at different conditions to generate cycles to failure data in Weibull plots.

CONCLUSIONS

- Ball/package failure shear forces were much lower for CSPs than BGAs. In general, forces increased after isothermal aging at 100°C to 1,000 hours, and then leveled off or slightly decreased to 2,000 hours. For aging at 125°C to 1,000 hours, for a few cases, forces dropped by 40% and then leveled off or decreased to 2,000 hours.
- Traditionally, solder joint failure was considered to be the weakest link in the microelectronics attachment reliability. This might not be true for CSPs with innovative designs and the use of new materials and processes. For example, the internal package TAB lead bond failure was considered to be the possible cause of a CSP failure after cycling.
- The solder joints which were reflowed twice, in a double sided assembly, showed earlier failures. For a leadless package, this was further worsened by package back to back (mirror image) assembly.

Visual inspection has been standard practice for characterizing solder joint quality for providing rejection criteria for nonconformance to specification for aerospace applications. Inspection for acceptance is still a major challenge for BGAs. The challenges are further magnified for the inspection of grid CSPs with smaller features in addition to hidden solder joints. Package internal failure also raises other assurance issues.

Stringent process controls are acceptable for commercial, but additional joint integrity verification criteria are needed for high reliability applications. Joint integrity verification is critical for space missions.

Furthermore, for CSP implementation, meaningful reliability data are needed. Accelerated thermal cycling might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analyses need to be performed to build confidence in assembly reliability. Thus, understanding the overall philosophy of qualification testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is the key to collecting meaningful test results and building confidence in its implementation.

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